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CONFIRMATION NO. 6568

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SERIAL NUMBER 10/624,833	FILING DATE 07/22/2003 RULE	CLASS 438	GROUP ART UNIT 2823	ATTORNEY DOCKET NO. 3572.2US (97- 1243.02/US)
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APPLICANTS

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** CONTINUING DATA *****

This application is a DIV of 09/917,127 07/27/2001 PAT 6,780,746 *now PAT 6,780,746*
 which is a DIV of 09/586,243 06/02/2000 PAT 6,717,245. *ME 8/24/04*

** FOREIGN APPLICATIONS *****

none ME

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

** 03/22/2004

Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	STATE OR COUNTRY ID	SHEETS DRAWING 3	TOTAL CLAIMS 6	INDEPENDENT CLAIMS 3
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	EXAMINER'S SIGNATURE <i>Michelle Estrada</i>	INITIALS <i>ME</i>		

Verified and
Acknowledged

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TITLE
Method for fabricating a chip scale package using wafer level processing and devices resulting therefrom

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